3D Packaging for Superconducting Qubits

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MIT-LL Quantum Information and Integrated Nanosystems Group

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Computing Development Timeline

Classical (Electronic) Computing

- Vacuum tube (1906)
- ENIAC (1946)
- Transistor (1947)
- TX-0 (1956)
- Integrated circuit (1958)
- 2k transistors (1971)
- 5.5M transistors (1995)
- Pentium Pro (1995)
- 5.5B transistors (2014)
- Xeon Haswell (2014)
- 32 cores (2017)
- 2k transistors (1995)
- i4004 (1971)
- 18 cores (2014)
- 19.2B transistors (2017)

Quantum Computing

- Quantum simulator proposed (1981)
- Shor's algorithm (1994)
- Initial qubit experiments (1995-2005)
- Few-qubit processors & error detection (2012-2016)
- Cloud-based quantum computers (2017)
- 5µm
- SC qubits
- Ions

Quantum computing is transitioning from scientific curiosity to technical reality

- “Bigger science” & engineering (2015-present)
Potential value of quantum computing for economic and information security is driving significant worldwide investment – currently estimated at $100’s Million / year
Outline

- Introduction
- 3D integration Approach
- Superconducting multi-chip module (S-MCM)
- Flip-Chip Qubit
- Semiconductor Vs Superconducting Packaging
- Summary
Why is a Quantum Computer Potentially So Powerful?

<table>
<thead>
<tr>
<th>Logic element</th>
<th>Classical Computer</th>
<th>Quantum Computer</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>State</strong></td>
<td>“Bit”: classical bit (transistor, spin in magnetic memory, …)</td>
<td>“Qubit”: quantum bit (any coherent two-level system)</td>
</tr>
<tr>
<td></td>
<td>0 “Or” 1</td>
<td>Superposition: $</td>
</tr>
<tr>
<td><strong>Computing</strong></td>
<td></td>
<td>“phase”</td>
</tr>
</tbody>
</table>
| | N bits: *One of* $2^N$ possible N-bit states  
000, 001, …, 111 (N = 3) | N qubits: $2^N$ components to one state  
$\alpha|000\rangle + \beta|001\rangle + \ldots + \gamma|111\rangle$ (N = 3) |
| | Change a bit: *new calculation* (classical parallelism) | Quantum parallelism & interference |
| | ![Diagram of computing process] | ![Diagram of quantum computing process] |

Quantum computers encode information in a fundamentally different way than classical computers.
Quantum Race

Intel unveils 49-qubit superconducting chip
18 Jan 2018

Intel has announced the design and fabrication of a 49-qubit superconducting quantum-processor chip at the Consumer Electronics Show in Las Vegas. Speaking at the conferer Intel chief executive Brian Krzanich introduced “Tangle Lake”, a quantum-processor chip operated at extremely low temperatures. The device takes its name from the Tangle Lake frigid chain of lakes in Alaska, and is a nod to quantum entanglement.

Tangle Lake is designed to store and process quantum information in qubits that are superconducting circuits. Krzanich said that the chip is an important step towards developing quantum computers that could quickly solve mathematical problems involved in some of society’s most pressing issues – from drug development to climate forecasting.

Large-scale integration
He also announced progress in Intel’s research on spin qubits, which have qubits based on the spins of single electrons. While superconducting chips tend to be relatively large, spin-qubits can be miniaturized using well-established silicon-chip fabrication processes. This means that it may be possible to manufacture quantum processors containing large numbers of spin qubits. This large-scale integration would be could be more difficult for

Visual credit: Armit and Amara SH4, ZIL, Intel 2019. The name Quantum Machine is taken over from the best classical supercomputer. The quantum computer is a very effective way to do quantum computations. Quantum supremacy has been seen as a milestone for the future of quantum computers and supercomputers. Quantum computers use supercomputers and fast classical computers. It is shown that a quantum machine needs an expected amount of time to solve a complex problem. It looks like Google has given us the first experimental demonstration of quantum computing (an application). The scientific achievement is

Michelle Simmons, a quantum physicist at the University of New South Wales in Sydney, Added: The research first appeared in November by the New York Times and other outlets, after an early version of the paper was leaked to the website of NIST, which collaborates with Google on quantum computing, before being published in Nature. It appears the researchers did not confirm that it had invented the paper, nor would comment on the results. Although the calculation Google claims – checking the outcomes from a quantum computer does not require a supercomputer. "The scientific achievement is
**Qubit Quality**

**Gate time**: Time required for a single operation
- All computers require fast logical operations
- Classical processor: ~1 GHz (1 ns per operation)

**Coherence time**: The qubit’s lifetime

![Diagram of qubit states](image)

- Quantum state
- State decaying
- State lost

**Figure of Merit**: \( \frac{\text{Coherence time}}{\text{Gate time}} \)

Most lenient threshold for quantum error correction (to sustain computation): \( >10^3 \) operations per qubit lifetime
Develop 3D qubit integration process with the following attributes:

- Extensible approach
- Compatible with qubit design and fabrication
- Maintain qubit quality
Why 3D Integration Approach?

- Planar architecture: Increase qubit array by increasing chip size.
- 3D integration helps to integrate more qubits and connectivity by relegating the routing of readout and control lines to the third dimension.

Example: 1X5 transmon-style qubit array
Each qubit requires control bias lines and read out resonator

3D Integration Approach

- All Si Technologies
- Fabricate and optimize all layers/chips/devices separately
- Join sequentially and Interconnect with superconducting Indium bumps
3D Integration Approach

Monolithic Multilayer Wiring with Niobium Trilayer JJs

Qubit coherence limited to <100 ns due to lossy dielectrics

Flip-Chip Integration

Limited mitigation of interactions between qubits and routing-tier dielectrics

3-Tier Stack

Large qubit mode volume supports high connectivity and maintains high coherence

Qubit Tier

qubits and couplers

well separated (200 µm)

Superconducting Multichip Module

Interposer Tier

qubits and couplers

lossy dielectrics

Superconducting Multichip Module

Qubit Tier

qubits and couplers

lossy dielectrics

Superconducting Multichip Module

qubits and couplers

lossy dielectrics
Advantages of 3D Integration Approach

- Qubits, interconnects, control circuits are optimized separately, independently.

- Access to dense wiring layers through the interposer that isolates qubits from lossy surfaces. Thick interposer provides large mode volume to reduce effects of surface losses.

- 3D integration with superconducting TSV interrupted resonator helps to reduce quantum circuit footprint/form factor.

- Possible to integrate best superconducting qubits and components. Possible to combine multiple technologies fabricated using different process.
Integration Scheme

**Individual tiers**
- Qubit Tier
- Interposer Tier
- Superconducting Multichip Module (SMCM) Tier

**Two-tier stack without TSVs**
- Qubit Tier
- Interposer Tier

**Two-tier stack with TSVs**
- Qubit Tier
- Interposer Tier

**3-tier stack**
- Qubit Tier
- Interposer Tier
- Superconducting Multichip Module (SMCM) Tier

**Enables:**
- Rapidly prototype designs
- Validate new fab capabilities
- Off-chip readout and control to reduce cross-talk
- Increased routing and JJ complexity
- Additional routing complexity
- Prototype three-tier stack
- High density interconnects
- Trilayer JJs for additional circuit complexity

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Rabindra N. Das - 14 May 2021

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Hirjibehedin, Yost, Yoder, *et al.*, *in preparation* (2021)

Key Demonstration for Qubits

Six Identical Qubits Coupled to Quarter Wave Resonators

Packaged Qubit with Flip-Chip Bonded on Top

- Characterized effects of proximity of Si surface
- Established low-resistance interconnect path between interposer and Qubit chip.
- Demonstrated capacitive coupling between interposer and qubit chip
- Demonstrated inductive coupling between interposer and qubit chip

Demonstrated Key Flip-Chip Bonding Building Blocks

- Proximal surface
- Electrical conduction
- Capacitive coupling
- Inductive coupling

Qubit Flip-Chip Characterization

- Alignment, bonding and parallelism:

IR transmission image of overlaid alignment fiducials within ± 1 µm post-bond

Confocal image for Parallelism

X-ray for bonding optimization

Qubit loop to off-chip bias line alignment

Das, et al., IEEE ECTC 504-1414 (2018)
Indium Bump DC Resistance

Four-wire measurement of bump chain

Optical micrograph of one side of bump chain structure with 2,704 indium bumps

Confocal image of indium bumps

2,704 indium bumps connecting Al traces

Under bump metal
Ti/Pt/Au

Measured resistance of ~240 nΩ/bump at 10 mK, consistent with underbump metal (UBM) resistance

Effect of Flip-chip integration on Qubit Quality

Coherence times comparable to planar qubits of same design

Superconducting TSVs

Test structures for four-wire measurements of TSV chains

Cross-section of TSV lined with TiN

High-yield superconducting TSVs with $I_c > 10$ mA
($>20,000$ chain links measured)

Mallek, Yost, et al., *arXiv* (2021)
Reduce Form Factor

Cross-section of TSV lined with TiN

Superconducting TSV-integrated/ interrupted resonator reduces readout circuit area

Schwartz*, Hazard*, Woods*, et al., in preparation

Rosenberg, et al., IEEE Microwave 21:8, 72-86 (2020)
3-Tier Stack
Double Bump Bonding

Three interconnect stages between qubit and SMCM tiers

Qubit Tier
Interposer Tier
Superconducting Multichip Module

Double-Bump-Bonded 3-Tier Stack

Confocal and SEM 3-Tier Stack Images

Combines high-yield TSV and bump-bond processes to test full 3-tier stack

Das, et al., IEEE ECTC 504-1414 (2018)
Rosenberg, et al., IEEE Microwave 21:8, 72-86 (2020)
Hirjibehedin, Yost, Yoder, et al., in preparation (2021)
3-Tier Stack

DC Connectivity

Three interconnect stages between qubit and SMCM tiers

Qubit Tier

Interposer Tier

Superconducting Multichip Module

DC connectivity yield of 99.4% to 99.98% (across >6500 measured links)

*Normal UBM metal has low residual resistance

Rosenberg, et al., IEEE Microwave 21:8, 72-86 (2020)

Hirjibehedin, Yost, Yoder, et al., in preparation (2021)
3-Tier Stack

Qubit Performance

**Qubit tier**
- 5 C-shunt flux qubits

**Interposer tier**
- transmission line
- 10 resonators
- 10 local flux bias lines
- 5 C-shunt flux qubits

**SMCM tier**
- RF signal routing
- DC signal routing

3-tier stack qubit coherence times comparable to planar qubits of same design

Hirjibehedin, Yost, Yoder, et al., *in preparation* (2021)
Semiconductor Vs Superconductor Packaging

**Semiconductor Industry Trends**

- **2.5D Technology**
  - Package Interposer Package (PIP)
    - Das et al., IEEE ECTC 1333 (2012)
  - System-in-Package (SiP)
    - Das et al., IEEE ECTC 1593 (2012)

- **3D Technology**
  - Organic substrate
    - C4
    - BGA

**MITLL Superconductor Packaging**

- **Superconducting Multichip module (S-MCM)**
  - 16 chip S-MCM

**HBM Technology**

- **µ-bump**
  - Cu post with solder tip

- **µ-bump pitch**
  - 45µm
  - 35µm

- **No of µ-bump assembly**
  - 1
  - 2

- **Maximum chips**
  - 5
  - 4 (20X20 mm²)
  - 16 (5X5 mm²)

- **Size**
  - Interposer area ~750 mm²
  - MCM area ~9200 mm²

- **Feature size**
  - 0.4µm
  - 0.8µm

**Future Efforts**

- **3D integrated re-workable package**
- **3D integrated rigid-flex package**

### Technology Comparison

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<th>Technology</th>
<th>2.5D</th>
<th>S-MCM</th>
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<tr>
<td>µ-bump</td>
<td>Cu post with solder tip</td>
<td>Indium</td>
</tr>
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**References**

A look into the Future: 3D Quantum Vision

Double bump bonding

High Quality Qubit
Off chip coupling
Superconducting TSVs

Travelling-wave parametric amplifiers

Flip-chip: 16 chip S-MCM

Future Path

Hirjibehedin, Yost, Yoder, et al., in preparation (2021)
Yost, Schwartz, Mallek, et al., npj Quantum Information (2020)

Das, et al., IEEE ECTC 504-1414 (2018)
Rosenberg, et al., IEEE Microwave 21:8, 72-86 (2020)
Summary

• An integrated approach to develop 3D constructions on various flip-chip qubit package configurations is demonstrated.

• 3-tier stack enhances connectivity and functionality while maintaining Qubit performance.

• Rigid-flex technology may be attractive for connecting superconducting qubit module to routing, control or amplification circuits.
Superconducting Multi-Chip Module (S-MCM)

Superconducting chip: 5mmX5mm

- 2 chip S-MCM
- 4 chip S-MCM
- 16 chip S-MCM

High-yield superconducting MCMs (Fabricated up to 96mmX96mm S-MCM)

Large Superconducting Chip Integration
(Thermocompression bonding capability)

S-MCM: 32mm x 32mm
16 (5mm x 5mm) chips

MCM: 48mm x 48mm
2 (20mm x 20mm) chips